IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: **Shannon, et al.**	§	Serial No.: **10/823,371**
Filed: **April 12, 2004**	§	Confirmation No.: **4850**
Docket No.: **8824/ETCH/DRIE**	§	Group Art Unit: **1792**
	§	Examiner: **Arancibia, Maureen G.**
For: **DUAL FREQUENCY RF MATCH**	§	

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

REPLY BRIEF

In response to the Examiner's Answer dated on November 13, 2008, the Appellants hereby submit this Reply Brief to the Board of Patent Appeals and Interferences. The Appellants believe that no fees are due in connection with this submission. However, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 50-3562 for any fees required to make this response timely and acceptable to the Office.

REAL PARTY IN INTEREST

The real party in interest is Applied Materials, Inc., located in Santa Clara, California.

RELATED APPEALS AND INTERFERENCES

The Appellants know of no related appeal and/or interference that may directly affect or be directly effected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1, 3-10, and 12-21 are pending in the application. Claims 2 and 11 have been cancelled. Claims 1, 3-10, and 12-21 stand rejected as discussed below. All rejections of claims 1, 3-10, and 12-21 as set forth in the Final Office Action dated April 1, 2008, and as noted below, are appealed. The pending appealed claims are shown in the attached Appendix.

STATUS OF AMENDMENTS

All claim amendments have been entered by the Examiner. No amendments to the claims were proposed after the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Embodiments of the present invention relate to match circuits for coupling two RF signals to an electrode in a plasma enhanced semiconductor processing chamber. In embodiments corresponding to independent claim 1, an apparatus (108) for matching the impedance of a pair of RF sources (104, 106) coupled to a single electrode (110) to the impedance of a plasma in a semiconductor substrate processing chamber (100) includes a first sub-circuit (202) for matching the impedance of a first variable frequency RF signal generated by a first RF source to the impedance of the plasma; and a second sub-circuit (204) for matching the impedance of a second variable frequency RF signal generated by a second RF source to the impedance of the plasma, the second sub-circuit connected to the first sub-circuit to form a common output (212) that is coupled to the electrode; wherein the first and second sub-circuits each further comprise at least

one fixed set of series components (*e.g.*, L_1, C_2, or L_2, C_3) and at least one variable shunt component (*e.g.*, C_1 or C_4) connected to ground, and wherein a first match tune space defined by the first sub-circuit can be varied without affecting a second match tune space defined by the second sub-circuit. (*Specification*, ¶¶ [0014-0016] discussing Fig. 1; ¶¶ [0017] and [0019] discussing Fig. 2; and ¶¶ [0020]-[0021] discussing Fig. 3.)

In embodiments corresponding to independent claim 9, an apparatus (108) for matching the impedance of a pair of RF sources (104, 106) coupled to a single electrode (110) to the impedance of a plasma in a semiconductor substrate processing chamber (100) includes a first sub-circuit (202) for coupling to a first variable frequency RF source and having a first set of fixed series components (*e.g.*, L_1, C_2) and a first variable shunt to ground (*e.g.*, C_1); and a second sub-circuit for coupling to a second variable frequency RF source and having a second set of fixed series components (*e.g.*, L_2, C_3) and a second variable shunt to ground (*e.g.*, C_4), the second sub-circuit connected to the first sub-circuit to form a common output (212) that is coupled to the electrode; wherein a first match tune space defined by the first sub-circuit can be varied without affecting a second match tune space defined by the second sub-circuit. (*Specification*, ¶¶ [0014-0016] discussing Fig. 1; ¶¶ [0017] and [0019] discussing Fig. 2; and ¶¶ [0020]-[0021] discussing Fig. 3.)

In embodiments corresponding to independent claim 10, an apparatus (108) for matching the impedance of a pair of RF sources (104, 106) coupled to a single electrode (110) to the impedance of a plasma in a semiconductor substrate processing chamber (100) includes a processing chamber (100) comprising at least a first electrode (110); a first variable frequency RF source (104); a second variable frequency RF source (106); and a dual frequency matching circuit (108), comprising: a first sub-circuit (202) coupled to the first RF source; and a second sub-circuit (204) coupled to the second RF source and connected to the first sub-circuit to form a common output (212) that is coupled to the first electrode; wherein the first and second sub-circuits each further comprise at least one fixed set of series components (*e.g.*, L_1, C_2, or L_2, C_3) and at least one variable shunt component (*e.g.*, C_1 or C_4) connected to ground, and wherein a first match tune space defined by the first sub-circuit can be varied without affecting a second match tune space defined by the second sub-circuit. (*Specification*,

¶¶ [0014-0016] discussing Fig. 1; ¶¶ [0017] and [0019] discussing Fig. 2; and ¶¶ [0020]-[0021] discussing Fig. 3.)

In embodiments corresponding to independent claim 19, an apparatus (108) for matching the impedance of a pair of RF sources (104, 106) coupled to a single electrode (110) to the impedance of a plasma in a semiconductor substrate processing chamber (100) includes a first sub-circuit (202) for matching the impedance of a first RF signal having a variable frequency of between about 50 KHz and about 14.2 MHz generated by a first RF source to the impedance of the plasma; and a second sub-circuit (204) for matching the impedance of a second RF signal having a variable frequency of between about 50 KHz and about 14.2 MHz generated by a second RF source to the impedance of the plasma, the second sub-circuit connected to the first sub-circuit to form a common output (212) that is coupled to the electrode, and wherein a first match tune space defined by the first sub-circuit can be varied without affecting a second match tune space defined by the second sub-circuit. (*Specification*, ¶¶ [0014-0016] discussing Fig. 1; ¶¶ [0017] and [0019] discussing Fig. 2; and ¶¶ [0020]-[0021] discussing Fig. 3.)

In embodiments corresponding to independent claim 21, an apparatus (108) for matching the impedance of a pair of RF sources (104, 106) coupled to a single electrode (110) to the impedance of a plasma in a semiconductor substrate processing chamber (100) includes a first sub-circuit (202) for matching the impedance of a first RF signal generated by a first RF source to the impedance of the plasma; and a second sub-circuit (204) for matching the impedance of a second RF signal generated by a second RF source to the impedance of the plasma, the second sub-circuit connected to the first sub-circuit to form a common output (21) that is coupled to the electrode; wherein the first and second sub-circuits are each adapted to vary a respective match tune space defined by the respective sub-circuit without affecting another respective match tune space defined by the other sub-circuit. (*Specification*, ¶¶ [0014-0016] discussing Fig. 1; ¶¶ [0017] and [0019] discussing Fig. 2; and ¶¶ [0020]-[0021] discussing Fig. 3.)

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3, 4, 6, 7, 9, 10, 12-15 and 17-21 stand rejected under 35 USC. §103(a) as being unpatentable over Japanese Application Publication No. 08-097199A, published April 12, 1996 to *Nishiyama et al.* (hereinafter *Nishiyama*) in view of Japanese Patent Application Publication No 06-243992, published September 2, 1994 to *Deguchi, et al.* (hereinafter *Deguchi*).

2. Claim 5 stands rejected under 35 USC §103(a) as being unpatentable over *Nishiyama* in view of *Deguchi* as applied to Claim 1 above, and further in view of US Patent No. 6,887,339, issued May 3, 2005, to *Goodman, et al.* (hereinafter *Goodman*).

3. Claims 8 and 16 stand rejected under 35 USC §103(a) as being unpatentable over *Nishiyama* in view of *Deguchi* as applied to Claims 1 and 10 above, and further in view of US Patent No. 6,641,149, issued November 4, 2003, to *Suemasa, et al.* (hereinafter *Suemasa*).

ARGUMENT

The following is provided solely in response to the comments made by the Examiner in the Response to Arguments section of the Examiner's Answer (*Examiner's Answer*, pp. 9-13.) The Appellants maintain all arguments and positions asserted in the prior-filed Appeal Brief in addition to any further comments and arguments made below.

CLAIM REJECTIONS

A. 35 USC §103 Claims 1, 3, 4, 6, 7, 9, 10, 12-15 and 17-21

The Appellants note that the Response to Arguments section of the Examiner's Answer is substantially the same as the Response to Arguments section of the Final Office Action dated April 01, 2008. The Appellants previously addressed these same arguments posed by the Examiner in the Appeal Brief dated September 2, 2008.

The only difference between the Response to Arguments section in the Examiner's Answer and that provided in the Final Office Action is apparently near the end of the Response to Arguments section, where the Examiner acknowledges the Appellants' position that the functional limitations of the claims impose further structural

limitations than asserted to be resultant from the combination of *Nishiyama* and *Deguchi*, but wonders what the further structural limitations may be. (Examiner's Answer, pp. 12-13.)

In response, the Appellants submit that the Examiner is ignoring the multitude of structural differences present in varying match circuit designs. For example, as recited in claim 1, the first and second sub-circuits each further comprise at least one fixed set of series components and at least one variable shunt component connected to ground, and wherein a first match tune space defined by the first sub-circuit can be varied without affecting a second match tune space defined by the second sub-circuit. Thus, the first and second sub-circuits are functionally limited by the further recitation that a first match tune space defined by the first sub-circuit can be varied without affecting a second match tune space defined by the second sub-circuit.

The Appellants note, for exemplary purposes only, the multitude of different combinations of elements that may be provided in different match circuits that would result in structural differences between the match circuits. For example, having different combinations of elements (*e.g.*, resistors, capacitors, inductors, or the like) or even similar elements having different values, each would result in a match circuit that is structurally different and that would have different capabilities.

As relevant here, the Appellants have noted that the cited art does not provide any indication that any combination of the cited art would have the same structure as functionally recited in the present claims. The Appellants have further noted that the Examiner's reliance on the Appellants' specification is insufficient to show any structural identity between the asserted combination of the cited art and the claims due to the lack of discussion in the present application as to how some other asserted combination of teachings may operate. To further this position, the Appellants have provided a declaration of the inventor that clearly demonstrated that matching circuits as presently claimed are structurally different than other matching circuits for coupling two frequencies to a common electrode and having at least one fixed set of series components and at least one variable shunt component connected to ground. Specifically, the declaration notes that "match circuit designs for coupling two frequencies to a common electrode and having at least one fixed set of series

components and at least one variable shunt component connected to ground may be designed that do not provide a first match tune space that can be varied without affecting a second match tune space." (Declaration of inventor Steven C. Shannon, filed September 27, 2007, ¶9.)

Thus, the Examiner's conclusion that the asserted combination is structurally identical to the limitations recited in the claims is clearly in error. Firstly, as pointed out in the example, above, the at least one fixed set of series components and the at least one variable shunt component connected to ground may have numerous structural differences due to the type of component, number of components, and respective value of the components present. Moreover, these structural differences are clearly shown to affect the ability of a match circuit to perform certain functions, and in particular, the functional limitations recited in the present claims. Specifically, the inability of certain match circuit configurations having at least one fixed set of series components and at least one variable shunt component connected to ground to provide independent tune space matching, as shown in the Declaration of Steven C. Shannon, clearly shows that the combination of cited art cannot inherently possess the same structure as the recited claims. This evidence further proves the Examiner's reliance on a theory of inherency – that the structure of the asserted combination of cited art is inherently structurally capable of performing the limitations recited in the claims – is also in error, as the allegedly inherent characteristic (the tune space independence) clearly does not necessarily flow from the asserted combination of cited art.

Thus Appellants maintain a *prima facie* case of obviousness has not been established as the combination of the cited art fails to teach, suggest, or otherwise yield the limitations recited in the claims.

Therefore, claims 1, 9, 10, 19, and 21, and all claims depending therefrom, are patentable over *Nishiyama* in view of *Deguchi*. Accordingly, the Appellants respectfully request that the rejection be withdrawn and the claims allowed.

B. 35 USC §103 Claim 5

For at least the reasons discussed above, the Appellants maintain that independent claim 1, from which the above rejected claim depends, recites limitations not taught or suggested by any combination of the cited references.

Thus, the Appellants maintain that claim 5 is patentable over *Nishiyama* in view of *Deguchi*, and further in view of *Goodman*. Accordingly, the Appellants respectfully request that the rejection be withdrawn and the claim allowed.

C. 35 USC §103 Claims 8 and 16

For at least the reasons discussed above, the Appellants maintain that independent claims 1 and 10, from which the above rejected claims respectively depend, recite limitations not taught or suggested by any combination of the cited references.

Thus, the Appellants maintain that claims 8 and 16 are patentable over *Nishiyama* in view of *Deguchi*, and further in view of *Suemasa*. Accordingly, the Appellants respectfully request that the rejection be withdrawn and the claims allowed.

CONCLUSION

For the reasons advanced above, Appellants respectfully urge that the rejections of claims 1, 3-10, and 12-21 as being unpatentable under 35 U.S.C. §103 are improper. Reversal of the rejections in this appeal, and allowance of all pending claims, is respectfully requested.

Respectfully submitted,

January 13, 2009

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CLAIMS APPENDIX

1. (Previously Presented) Apparatus for matching the impedance of a pair of RF sources coupled to a single electrode to the impedance of a plasma in a semiconductor substrate processing chamber, comprising:

a first sub-circuit for matching the impedance of a first variable frequency RF signal generated by a first RF source to the impedance of the plasma; and

a second sub-circuit for matching the impedance of a second variable frequency RF signal generated by a second RF source to the impedance of the plasma, the second sub-circuit connected to the first sub-circuit to form a common output that is coupled to the electrode;

wherein the first and second sub-circuits each further comprise at least one fixed set of series components and at least one variable shunt component connected to ground, and wherein a first match tune space defined by the first sub-circuit can be varied without affecting a second match tune space defined by the second sub-circuit.

2. (Cancelled)

3. (Previously Presented) The apparatus of claim 1, wherein a match tune space of the first and second RF sources is controllable by the shunt components.

4. (Previously Presented) The apparatus of claim 1, wherein a match tune space of the first and second RF sources is controllable by varying at least one of a first and a second frequency of a signal respectively generated by the first and second RF sources.

5. (Original) The apparatus of claim 1, wherein the first and second RF sources each have a 50 Ohm output impedance.

6. (Original) The apparatus of claim 1, wherein the first and second sub-circuits are fixed in a predetermined configuration prior to performing a particular process in the processing chamber.

7. (Original) The apparatus of claim 1, wherein the impedance of the first and second RF sources may be matched to the impedance of the processing chamber during processing by at least one of:

varying at least one value of a component of the first and second sub-circuits during operation of the processing chamber; or

varying the frequency of at least one of the first and the second RF sources.

8. (Original) The apparatus of claim 1, further comprising:

an isolation sub-circuit for preventing power supplied from either of the first and second RF sources from being coupled to the other of the first and second RF sources.

9. (Previously Presented) Apparatus for matching the impedance of a pair of RF sources coupled to a single electrode to the impedance of a plasma in a semiconductor substrate processing chamber, comprising:

a first sub-circuit for coupling to a first variable frequency RF source and having a first set of fixed series components and a first variable shunt to ground; and

a second sub-circuit for coupling to a second variable frequency RF source and having a second set of fixed series components and a second variable shunt to ground, the second sub-circuit connected to the first sub-circuit to form a common output that is coupled to the electrode;

wherein a first match tune space defined by the first sub-circuit can be varied without affecting a second match tune space defined by the second sub-circuit.

10. (Previously Presented) Apparatus for matching the impedance of a pair of RF sources coupled to a single electrode to the impedance of a plasma in a semiconductor substrate processing chamber, comprising:

a processing chamber comprising at least a first electrode;

a first variable frequency RF source;

a second variable frequency RF source; and

a dual frequency matching circuit, comprising:

a first sub-circuit coupled to the first RF source; and

a second sub-circuit coupled to the second RF source and connected to the first sub-circuit to form a common output that is coupled to the first electrode;

wherein the first and second sub-circuits each further comprise at least one fixed set of series components and at least one variable shunt component connected to ground, and wherein a first match tune space defined by the first sub-circuit can be varied without affecting a second match tune space defined by the second sub-circuit.

11. (Cancelled)

12. (Previously Presented) The apparatus of claim 10, wherein a match tune space of the first and second RF sources is controllable by the shunt components.

13. (Previously Presented) The apparatus of claim 10, wherein a match tune space of the first and second RF sources is controllable by varying at least one of a first and a second frequency of a signal respectively generated by the first and second RF sources.

14. (Original) The apparatus of claim 10, wherein the first and second sub-circuits are fixed in a predetermined configuration prior to performing a particular process in the processing chamber.

15. (Previously Presented) The apparatus of claim 10, wherein the impedance of the first and second RF sources may be matched to the impedance of the processing chamber during processing by at least one of:

varying at least one value of a component of the first and second sub-circuits during operation of the processing chamber; or

varying the frequency of at least one of the first and the second RF sources.

16. (Original) The apparatus of claim 10, wherein the dual frequency matching circuit further comprises:

an isolation sub-circuit for preventing power supplied from either of the first and second RF sources from being coupled to the other of the first and second RF sources.

17. (Previously Presented) The apparatus of claim 1, wherein the first sub-circuit and the second sub-circuit are both configured to match the impedance of an RF signal having a frequency of between about 50 KHz and about 14.2 MHz.

18. (Previously Presented) The apparatus of claim 10, wherein the first RF source and the second RF source are both configured to provide an RF signal having a frequency of between about 50 KHz and about 14.2 MHz.

19. (Previously Presented) Apparatus for matching the impedance of a pair of RF sources coupled to a single electrode to the impedance of a plasma in a semiconductor substrate processing chamber, comprising:

a first sub-circuit for matching the impedance of a first RF signal having a variable frequency of between about 50 KHz and about 14.2 MHz generated by a first RF source to the impedance of the plasma; and

a second sub-circuit for matching the impedance of a second RF signal having a variable frequency of between about 50 KHz and about 14.2 MHz generated by a second RF source to the impedance of the plasma, the second sub-circuit connected to the first sub-circuit to form a common output that is coupled to the electrode, and wherein a first match tune space defined by the first sub-circuit can be varied without affecting a second match tune space defined by the second sub-circuit.

20. (Previously Presented) The apparatus of claim 19, wherein the first and second sub-circuits each further comprise:

at least one fixed set of series components; and

at least one variable shunt component connected to ground.

21. (Previously Presented) Apparatus for matching the impedance of a pair of RF sources coupled to a single electrode to the impedance of a plasma in a semiconductor substrate processing chamber, comprising:

a first sub-circuit for matching the impedance of a first RF signal generated by a first RF source to the impedance of the plasma; and

a second sub-circuit for matching the impedance of a second RF signal generated by a second RF source to the impedance of the plasma, the second sub-circuit connected to the first sub-circuit to form a common output that is coupled to the electrode;

wherein the first and second sub-circuits are each adapted to vary a respective match tune space defined by the respective sub-circuit without affecting another respective match tune space defined by the other sub-circuit.

EVIDENCE APPENDIX

[NONE]

RELATED PROCEEDINGS APPENDIX

[NONE]